

# **SPI**

**Implementation in the IQRF platform**

## **User's Manual**



**Simple way to smarter wireless solutions**

## SPI Overview:

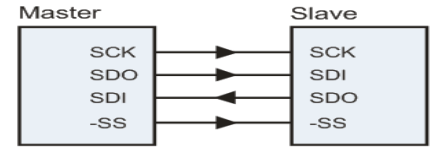
IQRF transceiver modules can communicate with external peripherals via the SPI interface.

SPI™ (Serial Peripheral Interface, introduced by Motorola) is a standard serial four wire synchronous data bus that can operate in full duplex. Devices communicate in master/slave mode with a single master initiating data frames. Multiple slave devices are allowed with individual slave select lines.

The **SPI bus** specifies four logic signals:

The SPI bus with a single slave:

SPI signal	TR pin	function	
<b>SCK</b>	C6	Serial Clock	issued by master
<b>SDI</b>	C7	Serial Data In	
<b>SDO</b>	C8	Serial Data Out	
<b>-SS</b>	C5	Slave Select	issued by master, active low



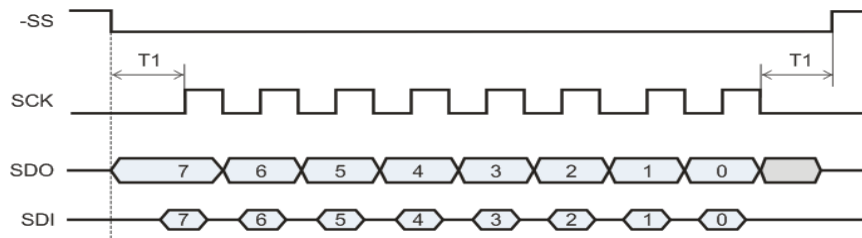
The IQRF transceiver modules can communicate as SPI slaves. Full as well as half duplex is supported. The SPI protocol is implemented in IQRF operating system. Thanks to the state machine architecture the communication is fully synchronous without any timeouts. It is packet oriented and works in OS background. Packets consist of selectable number of bytes (0 to  $N_{max}$ ). In time constrained cases the communication can be slowed down to work in OS foreground with longer delays between individual bytes. Data stream can even be suspended at all and continue at any time later.

The TR modules operate according the following **slave specification**:

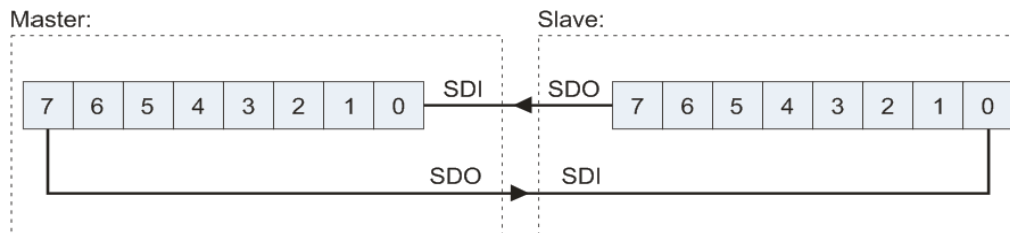
<b>Slave select</b>	Active low
<b>Idle clock polarity</b>	Low
<b>Clock edge</b>	Output data on falling SCK edge

**Data transfer** (from the slave point of view):

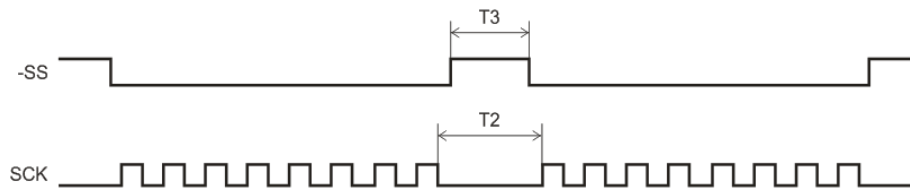
To start the communication, the master pulls the Slave select low. Then the master must wait for at least the  $T_1$  period before starting to issue clock cycles. During each SPI clock cycle, a duplex data bit can be transmitted to complete a full duplex byte transmission in 8 clocks.



Data is transferred using two internal shift registers to form a circular buffer, MSb first. After the registers have been shifted, the master and slave have swapped register values.



If there is more data to swap, the shift registers are loaded with new data and the process repeats. The master must wait for at least the  $T_2$  period before sending next byte. Deactivating the Slave Select for the  $T_3$  period between bytes is necessary.

**Timing:**


<b>SCK</b>	SPI clock	250 kHz	max.
<b>T1</b>	-SS to SCK, SCK to -SS	10 $\mu$ s	min.
<b>T2</b>	delay between bytes	100 $\mu$ s 500 $\mu$ s – in Slow mode	min.
<b>T3</b>	-SS pulse between bytes	20 $\mu$ s	min.

For detailed information see datasheet of respective microcontroller.

**Example:** SPI configuration of PIC16F88 used as a master:

	7	6	5	4	3	2	1	0
<b>SSPSTAT</b>	<b>SMP</b>	<b>CKE</b>	D/-A	P	S	R/-W	UA	<b>BF</b>
	0	1	-	-	-	-	-	read only
<b>SSPCON</b>	<b>WCOL</b>	<b>SSPOV</b>	<b>SSPEN</b>	<b>CKP</b>	<b>SSPM</b>			
	0	0	1	0	0	0	x	x

- SMP = 0 Input data sampled at middle of data output time.
- CKE = 1 Transmit occurs on transition from active to idle clock state.
- CKP = 0 Transmit on rising edge, receive on falling edge. Clock idle state is a low level.
- SSPM: SPI Master mode, clock timing (xx) depends on application.

**Packet structure:**

The master can send two types of packets with the following structure:

Master checks the SPI status of the module:

Master	<b>SPI_CHECK</b>
Slave	SPISTAT

Master reads/writes a packet from/to the module:

Master	<b>SPI_CMD</b>	PTYPE	DM <sub>1</sub>	DM <sub>2</sub>	---	DM <sub>SPIIDLEN</sub>	CRCM
Slave	SPISTAT	SPISTAT	DS <sub>1</sub>	DS <sub>2</sub>	---	DS <sub>SPIIDLEN</sub>	CRCS

Where:

SPI\_CHECK = 0x00

SPI\_CMD = 0xF0

SPISTAT: SPI status of the module

hex value	SPI status
00	SPI not working (disabled by the disableSPI() command)
07	SPI suspended by the stopSPI() command
3F	SPI not ready (buffer full, last CRCM O.K.)
3E	SPI not ready (buffer full, last CRCM error)
40 to 63	SPI data ready. Value - 0x40 = number of bytes to be sent from the slave (1 to N <sub>max</sub> )
80	SPI ready (communication mode)
81	SPI ready (programming mode)
82	SPI ready (debugging mode)
83	SPI not working in background (e.g. during receiving of RF packet) – Slow mode Master should prolong the delay between individual bytes when this status is received. See the T2 parameter in the table above.
FF	SPI not working (HW error)

SPI status of the module is indicated by the IQRF IDE when used together with related IQRF development tools (e.g. CK-USB-02):



PTYPE:

b7	b6	b5	b4	b3	b2	b1	b0
CTYPE		SPIDLEN					

CTYPE: communication type

10: full duplex (the master reads/writes from/to the module, bufferCOM changed)

00: half duplex (the master reads from the module, bufferCOM unchanged)

SPIDLEN: data length (from 1 to N<sub>max</sub>)

TR-xxx-xxA: N<sub>max</sub> = 35

TR-xxx-xxB: N<sub>max</sub> = 35

DM: data from the master

DS: data from the slave

CRCM = SPI\_CMD xor PTYPE xor DM<sub>1</sub> xor DM<sub>2</sub> ... xor DM<sub>SPIDLEN</sub> xor 0x5F

CRCS = PTYPE xor DS<sub>1</sub> xor DS<sub>2</sub> ... xor DS<sub>SPIDLEN</sub> xor 0x5F

**IQRF OS functions** related to SPI:

<code>void enableSPI()</code>	<i>Enables SPI communication. Hardware of the microcontroller is configured for SPI, related pins can not be used as general I/Os.</i>
<code>void disableSPI()</code>	<i>Disables SPI communication. SPI HW module of the microcontroller is switched off, related pins are general I/Os.</i>
<code>void startSPI(length)</code>	<i>Starts SPI packet transmission. This operates in OS background except of the Slow mode case.</i>
<code>void stopSPI()</code>	<i>Suspends SPI communication. It can continue at any time later (after another <b>startSPI</b> command)</i>
<code>bit getStatusSPI()</code>	<i>Updates SPI flags and packet length and checks whether SPI is busy</i>

**SPI flags:** available in `param2`

bit 7			bit 4	bit 3	bit 2		bit 0
-	-	-	<code>_SPICRCok</code>	<code>_SPIRX</code>	-	-	-

- `_SPIRX`      Something received on SPI.
- `_SPICRCok`    The last received SPI CRCM was O.K.

**SPI data length:** available in `param1`

**Caution:** SPI data length and SPI flags are copied to `param1` and `param2` (parameters used by OS functions) after the `getStatusSPI` command. They are only valid until another OS command using these parameters is called.

**Application:**

See IQRF OS User's manual, Application examples, [www.iqrf.org](http://www.iqrf.org) and [www.iq-esupport.com](http://www.iq-esupport.com).

**Document history:**

- 080516      First release
- 090427      `_SPIbusy` and `_SPIwrite` flags not documented. Use `getStatusSPI()` instead of `_SPIbusy`.

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# Sales and Service

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